

FIG. 1

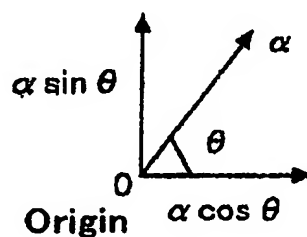
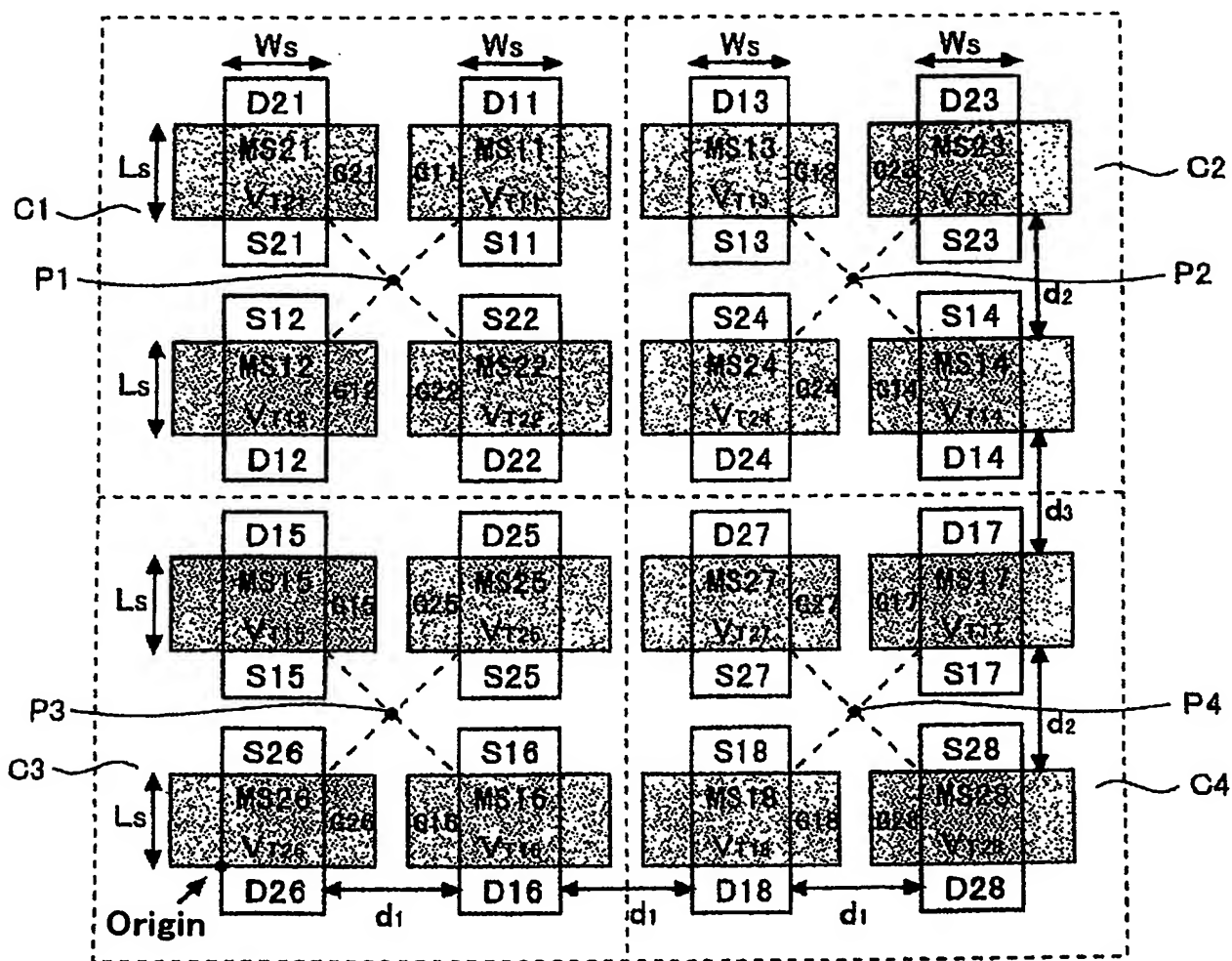


Figure 1 is a schematic diagram of a 32-bit parallel adder. It consists of two 16-bit adders, M1 and M2, each enclosed in a dashed oval. Adder M1 has inputs G1 and S1, and outputs D1 and S1. Adder M2 has inputs G2 and S2, and outputs D2 and S2. The carry propagation is shown as a chain of carry signals from G1 to G2. The equations $W_1 = W_s + W_s + W_s + W_s + W_s + W_s$ and $L_1 = L_s$ are shown for the first adder, and $W_2 = W_s + W_s + W_s + W_s + W_s + W_s$ and $L_2 = L_s$ for the second adder.

FIG.3

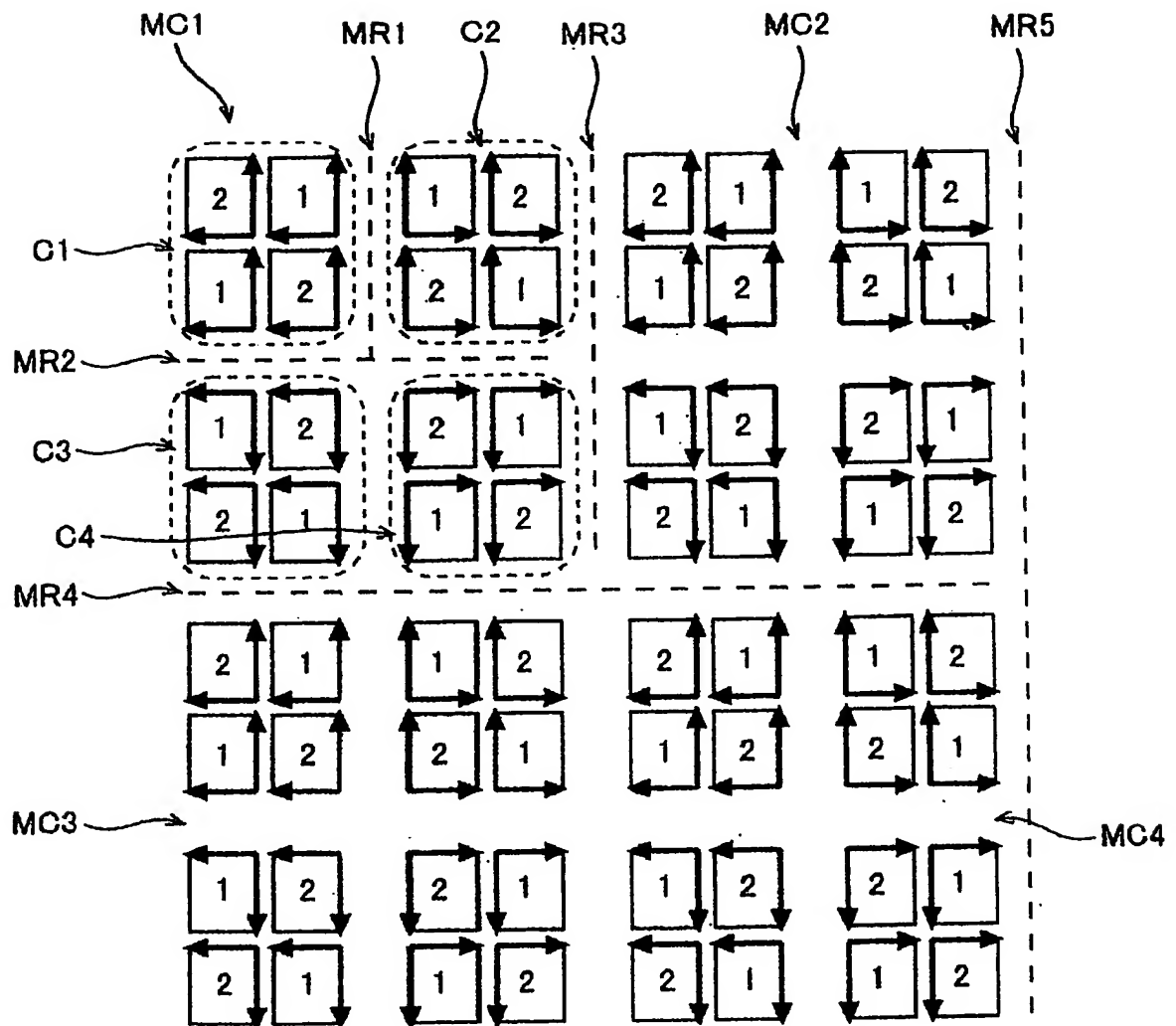


FIG.5

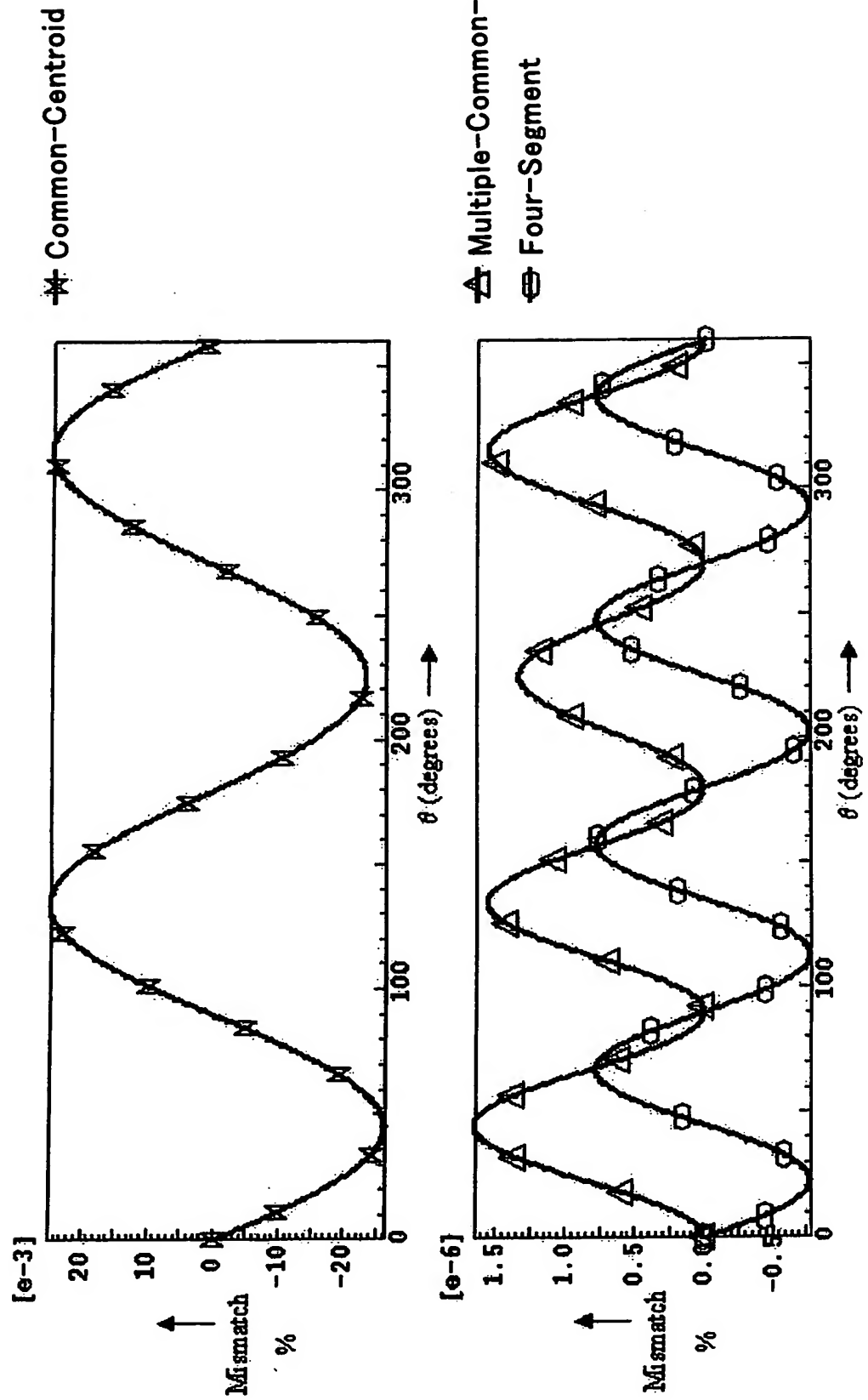


FIG. 6

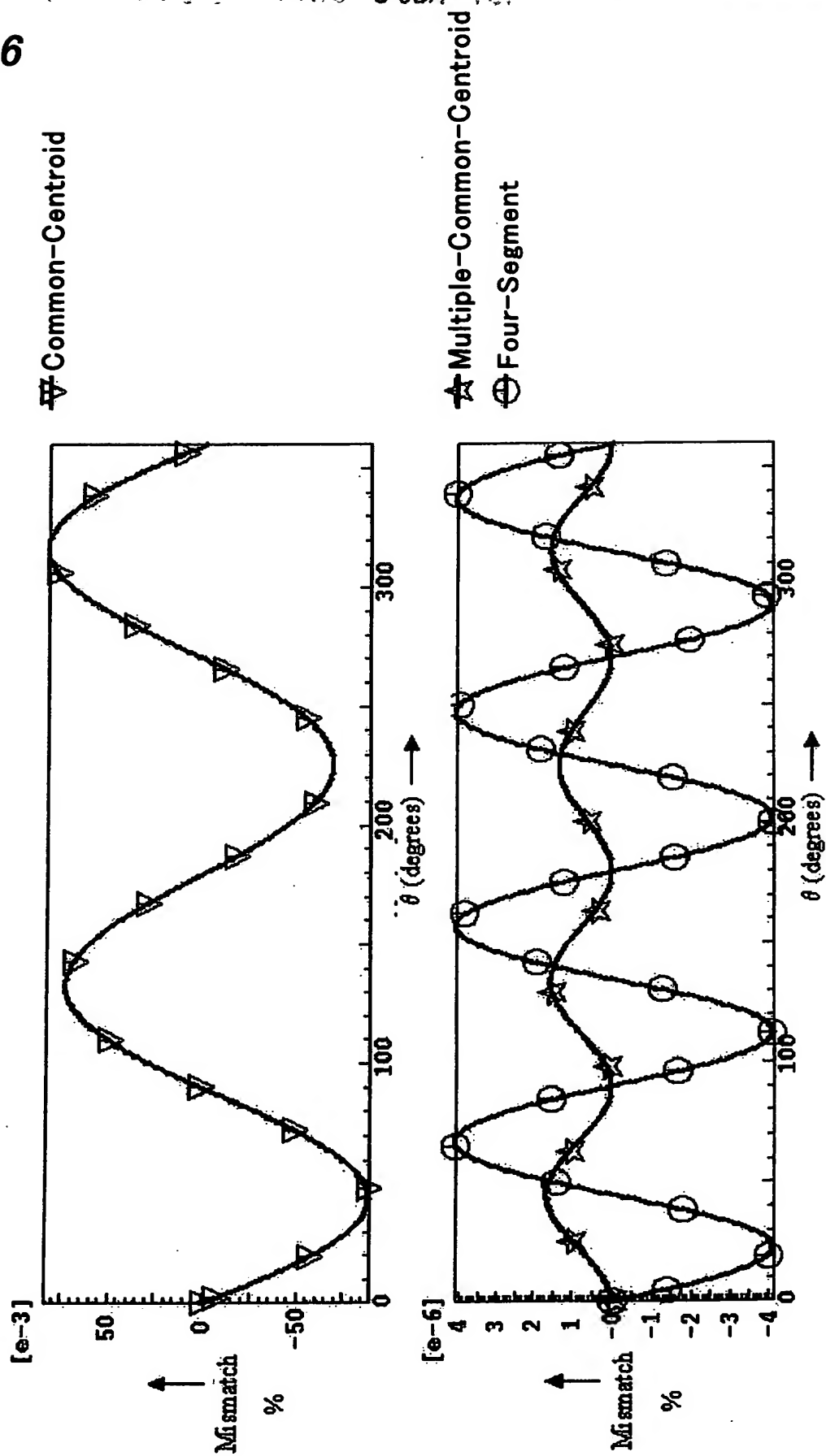


FIG. 7

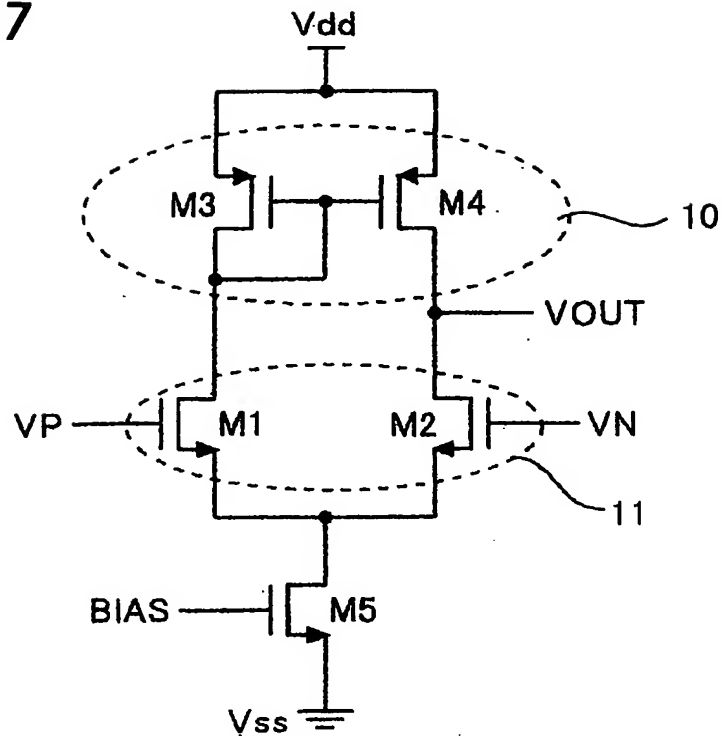


FIG. 8

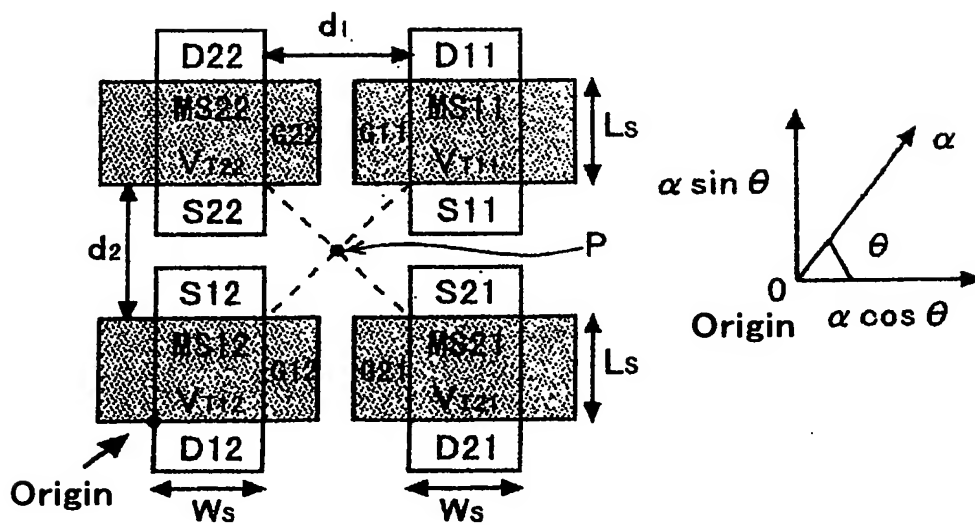


FIG. 9

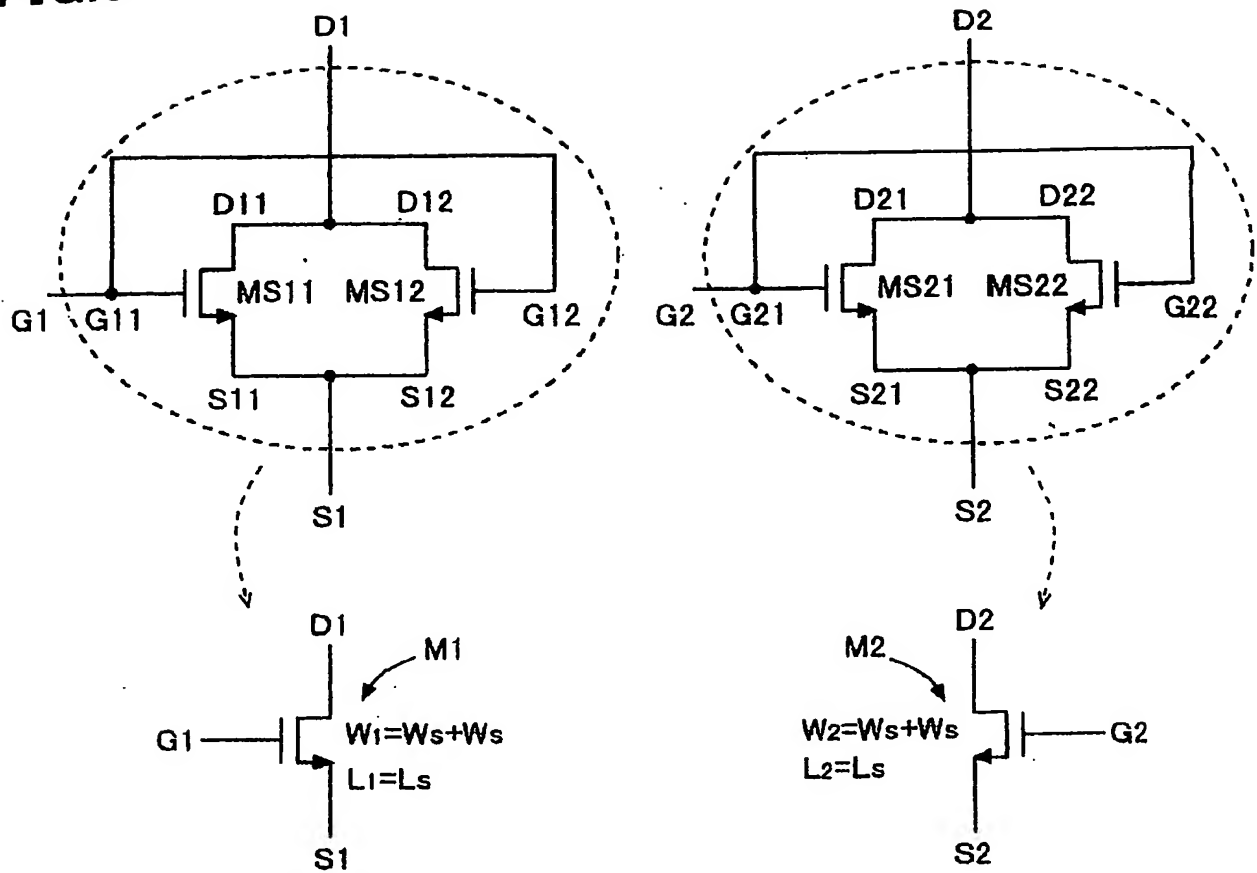


FIG. 10

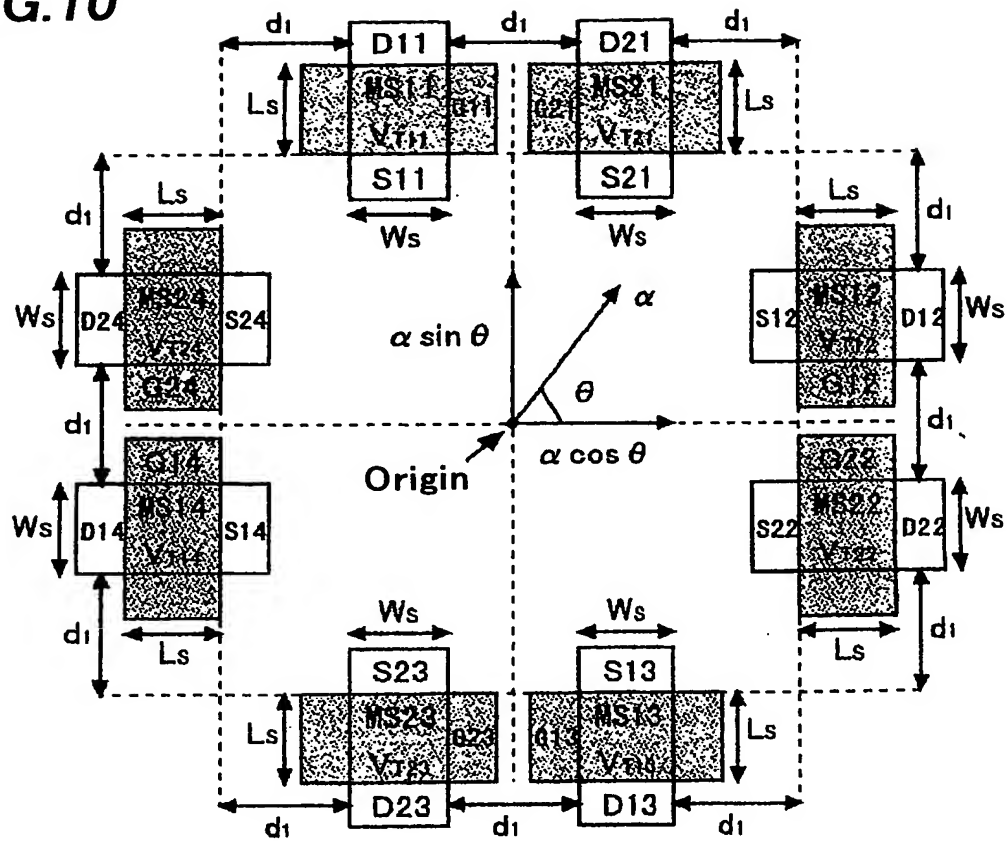


FIG. 11

